ABSTRACT OF THE DISCLOSURE

Concurrently formed self-aligned silicides on word lines and contacts of a memory device facilitate reduced resistance and/or reduced device sizing. The word-line silicide is formed at a stage significantly later than in standard processing, decreasing concerns of thermal stability of the silicide, thus allowing the use of lower-resistance silicides. In addition, by forming contacts to drain and/or source regions prior to forming the silicide for the word lines, aspect ratios for the contact holes or trenches are reduced for a given pitch, thus improving effectiveness of processing to remove material from these holes and trenches or allowing the use of a smaller pitch. By providing a process for the application of a silicide in array source interconnects, a single array source interconnect can couple an entire row of memory cells, thereby reducing the number of contacts made to an array ground.